

Digital microelectronic circuit with a clocked data-processing unit and a converting unit

The invention relates to a digital microelectronic circuit comprising a clocked data-processing unit and a converting unit which reads in the parallel data present at the output of the data-processing unit, performs a predetermined converting operation on the data and passes on the converted data.

5 In digital microelectronic circuits, data are usually manipulated synchronously, i.e. in a system clock. Successive processing units for serially processing data are usually clocked by the same clock in order that the serial processing steps can be performed in an orderly and synchronous way.

10 The drawback of such a successive arrangement of synchronous processing units is that the slowest processing unit predetermines the maximum allowable clock rate. Moreover, a processing unit may require a plurality of clock cycles for performing its data manipulation. In this case, the other processing units must wait for an equal number of clock cycles until they can start processing new data. The speed of the serial data processing with synchronous processing units is thus fixed by the slowest elements in two respects, namely
15 both in the applicable clock rate and in the data-processing rate (number of clocks required for a complete data manipulation).

An example of a serial synchronous data processing is the encryption or checking of data supplied by a primary data-processing unit such as a microprocessor (CPU). These data are typically secured against transmission errors or checked for transmission
20 errors by means of a method of serial procedures, for example, a CRC method (Cyclic Redundancy Check).

To increase the processing rate in serial data processing systems, it is known to use n different processing units with n different clock rates. For example, a converting unit may advantageously be operated with the multiple clock rate similarly as the other processing
25 units when it requires less time for performing a single clock than the other units and when it requires more clocks than the other processing units for completing the data manipulation. In this way, a certain acceleration of the overall processing in a system can be achieved in a system with fast serial synchronous processes and relatively slow synchronous processes. The availability of two or more different clock systems leads, however, to problems in

generating the clocks. Particularly, it may lead to disturbances due to superimposed clocks. Moreover, speed limits in the overall processing may result from a limited maximal clock so that the speed of the procedure does not predetermine the maximum possible processing speed.

5 Based on this background, it is an object of the present invention to improve a digital microelectronic circuit of the type described in the opening paragraph in such a way that an increase of the overall processing rate of data is obtained in a simple manner.

 This object is achieved with a circuit as defined in the characterizing part of claim 1.

10 The digital microelectronic circuit comprises at least one system-clocked data-processing unit such as, for example, a microprocessor, as well as a converting unit which reads in the data present at the output of the data processing unit, performs a predetermined converting operation on these data and passes on the data thus converted. The circuit is characterized in that the converting unit is realized in an asynchronous logic circuit, such that
15 the period of time for performing the converting operation in this logic circuit is shorter than the shortest time interval to the next change of the data present at the output of the data-processing unit.

 In the circuit according to the invention, a serial processing of data is performed with synchronous, clocked units and asynchronous, unclocked units. Although the
20 processing units are not synchronized on the basis of a common clock, an ordered, serial processing of the data can nevertheless be achieved in that the processing speed of the asynchronous logic is realized in a given manner with a view to the other units. The condition imposed on the processing speed of the asynchronous logic is that the period of time for performing a converting operation with data present at the input is shorter than the shortest
25 possible time interval to the next change of the data present at the output of the data-processing unit. This condition is particularly complied with when the maximum duration of the converting operation regarding all data in question is shorter than the minimum time interval between the change of data at the output of the data-processing unit. Said conditions ensure that the converting operation by the asynchronous logic is terminated when new data
30 for conversion are present at the output of the data-processing unit.

 In an embodiment of the circuit according to the invention which is particularly relevant in practice, the converting operation is an encryption and/or checking operation in the converting unit. Preferably, this may be a CRC method. The execution of such a method requires a proportionally large number of clock cycles in a synchronous logic,

so that the performance of this method reduces the overall processing speed of the data in a prior-art synchronous system. On the other hand, for example, a CRC method can be realized with a small logic gate depth so that it can be carried out at a high speed in an asynchronously operating converting unit.

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The invention will hereinafter be described by way of example with reference to the sole Figure. The Figure shows diagrammatically a digital microelectronic circuit with two processing units, namely a digital microprocessor (CPU) 1 and a converting unit 2. Data which are parallel present at the output of the data-processing unit 1 are to be checked by the converting unit 2 by means of a serial encryption method. For example, a CRC-32 method CPU op-code may be performed in the converting unit 2.

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The data-processing unit 1 is connected to a clock signal connection 3 for transmitting the system clock CLK. In conventional systems, the converting unit 2 would also be connected to the clock signal connection 3 so as to be able to operate synchronously with the data-processing unit 1. However, for a synchronous serial processing, the encryption of a plurality of clock periods would be required before the next parallel data word could be processed. Under circumstances, this would lead to considerable waiting times in the parallel data-processing operation.

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According to the invention, the converting unit 2 is therefore realized by means of an asynchronous logic so that it operates independently of the system clock on the connection 3. The converting operation to be performed nevertheless takes place at a high speed because processes with a small logic gate depth can be run considerably faster than are predetermined by the system frequency. The serial encryption by means of an asynchronous logic can be performed so quickly that it is terminated before new data are made available by the data-processing unit 1. The overall procedure of serial data processing is therefore not disturbed by the fact that the converting unit 2 operates asynchronously.

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The system shown in the Figure provides, for example, the possibility of asynchronously performing a CRC-32 encryption in two system clock periods of a 16 MHz clock processor. When the data to be recorded are available every two clock periods, a quasi-parallel encryption from the point of view of the data-processing unit 2 is obtained.

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Due to the embodiment of the circuit according to the invention, fast, serial synchronous processes can thus be parallelized from the point of view of the slow

synchronous system in synchronous systems which are slow relative thereto by using asynchronous logics, without a further high-frequency clock system being required.

The converting unit 2 passes the conversion results on to a subsequent unit at its input/output 6. Alternatively, it may also pass on the asynchronously computed results via the connection 5 to the CPU 1 for further processing. Similarly, it is possible for the converting unit 2 to receive its input data via the connection 6.

In addition to the CRC or CRC-32 methods, other examples of the function of the converting unit 2 are data compression, error correction, encryption methods, hash functions and the like.

- 10 Reference numerals:
- 1 data-processing unit CPU
 - 2 converting unit
 - 3 clock signal connection
 - 4, 5, 6 data connection